LISTING OF THE CLAIMS

A detailed listing of claims is presented below. Please amend currently amended claims as indicated below including substituting clean versions for pending claims with the same number. In addition, clean text versions of pending claims not being currently amended that are under examination are also presented. It is understood that any claim presented in a clean version below has not been changed relative to the immediate prior version.

1. (Cancelled)

2. (Currently Amended) A method for implementing a segmentation operation comprising the steps of:

providing a first segment selector for deriving a linear address of a segment descriptor in a first descriptor table,

providing a second segment selector for deriving a linear address of a segment descriptor in a second descriptor table,

attempting an access of the first descriptor table to derive a segment descriptor,

attempting an access of the second descriptor table to derive a segment descriptor if the access of the first descriptor table fails, and

storing a derived segment descriptor from a successful attempted access in a descriptor register;

and wherein any attempt to access is divided into discrete sub-steps comprising:

checking properties of a logical address to determine whether those properties are consistent with the criteria for addressing one of the first and

the second descriptor tables in a first discrete sub-step of deriving a linear address, and

performing a base-add operation to determine the linear address as a second discrete sub-step of deriving a linear address.

3. (Canceled) Please cancel Claim 3 without prejudice.

4. (Currently Amended) A microprocessor that implements a segmentation operation, comprising:

a first descriptor table ~~operable to store~~ for storing segment descriptors;

a second descriptor table ~~operable to store~~ for storing segment descriptors;

a first register ~~operable to hold~~ for holding a first segment selector operable to derive a linear address of a segment descriptor in the first descriptor table;

a second register ~~operable to hold~~ for holding a second segment selector operable to derive a linear address of a segment descriptor in the second descriptor table; and

a descriptor register ~~operable to store~~ for storing a derived segment descriptor from a successful attempted access of one of said first descriptor table and said second descriptor table;

wherein said microprocessor is operable for ~~to~~:

~~attempt~~ attempting an access of the first descriptor table to derive a segment descriptor;

if the access of the first descriptor table fails, ~~attempt~~ attempting an access of the second descriptor table to derive a segment descriptor; and

~~store~~ storing in the descriptor register a derived segment descriptor from a successful attempted access; and

wherein the microprocessor, further comprising:

a first base register for storing a first base address; and

a second base register for storing a second base address;

wherein said microprocessor is further operable to divide attempts to access into discrete sub-steps by:

checking properties of a logical address to determine whether those properties are consistent with criteria for addressing one of the first and the second descriptor tables in a first discrete sub-step of deriving a linear address; and

performing a base-add operation to determine the linear address as a second discrete sub-step of deriving a linear address, said performing including accessing a value from one of the first and the second base registers.

5. (Canceled) Please cancel without prejudice.